

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

**(19) World Intellectual Property
Organization
International Bureau**



(43) International Publication Date
6 January 2005 (06.01.2005)

PCT

(10) International Publication Number
WO 2005/001405 A1

(51) International Patent Classification⁷: G01K 15/00

(72) Inventors; and

(21) International Application Number:
PCT/IB2004/050957

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(22) International Filing Date: 22 June 2004 (22.06.2004)

(25) Filing Language: English

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(26) Publication Language: English

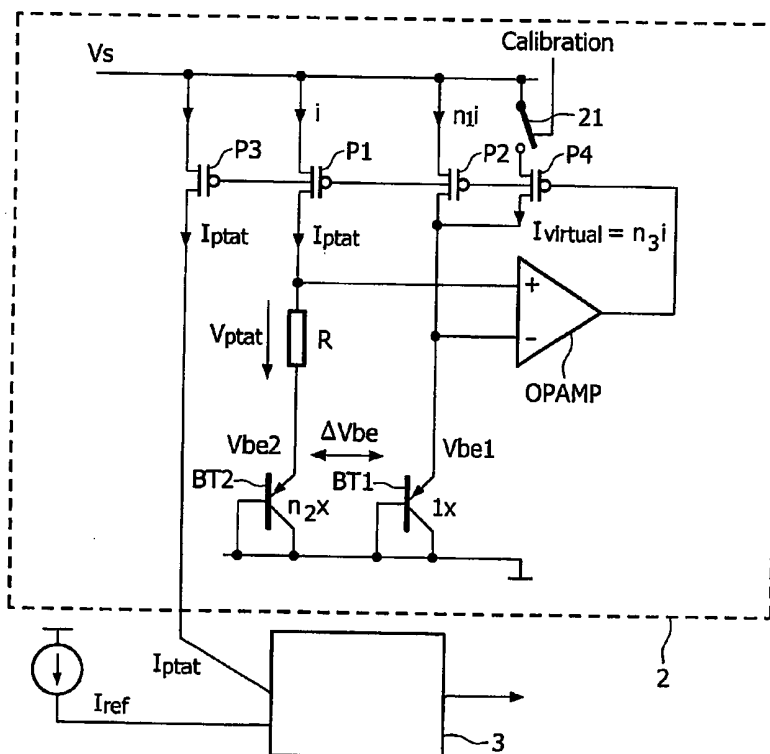
(81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MY, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM,

(30) Priority Data:
03101916.9 27 June 2003 (27.06.2003) EP

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(54) Title: METHOD AND ARRANGEMENT FOR TEMPERATURE CALIBRATION



(57) Abstract: The invention concerns an arrangement on a semiconductor chip for calibrating temperature setting curve having a signal generation unit (2) for providing a first signal ($I_{\text{ptat1}}, V_{\text{ptat1}}, f_{\text{ptat1}}$), which is proportional to the actual uncalibrated temperature T_1 of the chip. To avoid bringing the chip on a second temperature it is proposed to read a first signal ($I_{\text{ptat1}}, V_{\text{ptat1}}, f_{\text{ptat1}}$), which is proportional to the actual uncalibrated temperature T_1 of the chip and generate a signal offset ($I_{\text{virt}}, V_{\text{virt}}, f_{\text{virt}}$), which is combined with the first signal ($I_{\text{ptat1}}, V_{\text{ptat1}}, f_{\text{ptat1}}$) defining a second signal ($I_{\text{ptat2}}, V_{\text{ptat2}}, f_{\text{ptat2}}$) and to extract a first actual temperature T_1 from the first signal ($I_{\text{ptat1}}, V_{\text{ptat1}}, f_{\text{ptat1}}$) and a second uncalibrated temperature T_2 from the second signal ($I_{\text{ptat2}}, V_{\text{ptat2}}, f_{\text{ptat2}}$).



TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

(84) **Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI,

Published:

— with international search report

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